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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
AGGARWAL, YOGESH K	
ART UNIT	PAPER NUMBER
2622	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/680,239	PAIN ET AL.	
	Examiner	Art Unit	
	Yogesh K. Aggarwal	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-15,18 and 19* is/are allowed.

6)☒ Claim(s) *16 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/17/2006 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 16 and 17 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 16 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In this case, the newly recited limitation "wherein the linear integrator array of switched-capacitor integrators are arranged in rows and columns respectively equal to rows and columns of said linear sensing array" is not disclosed in the specification and therefore constitutes new matter. Figures 2a, 3a, 4a-b, 5a, 7a and 7b all show different embodiments of switched capacitor integrators (e.g. in figure 2a, See Page 15, line 14+, a total of n pairs of integrating capacitors C-

1 and C+1, C-2 and C+2, ..., C-n and C+n are coupled to the two differential outputs 212a and 212b to form the array of n integrators for that column) for a two dimensional array 110 and corresponding integrator array 120. There is no disclosure of a linear pixel array having a linear integrator array of switched-capacitor integrators that are arranged in rows and columns respectively equal to rows and columns of said linear sensing array. Although claim 16 was disclosed in original specification, the newly recited limitations constitute new matter.

Claim Objections

5. Claim 16 is objected to because of the following informalities: "wherein the linear integrator array of switched-capacitor integrators are arranged in rows and columns respectively equal to rows and columns of said linear sensing array" should be replaced by "wherein the linear integrator array of switched-capacitor integrators are arranged in a row and plurality of columns respectively equal to a row and columns of said linear sensing array". A linear array has only one row and multiple columns.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pettijohn et al. (US Patent # 5,149,954) and Aswell et al. (US Patent # 6,943,721).

[Claim 16]

Pettijohn et al. teaches a method comprising using a linear sensing array of pixels (fig. 1a shows a linear array comprising Va and Vb, col. 3 lines 3-8),

internally converting radiation-induced charge in each pixel into a voltage representing an electrical pixel signal (figure 1b discloses the output Va for each pixel, col. 3 lines 27-30),

coupling a linear integrator array of switched capacitor integrators (e.g. C1, C2, C3, C4, C5 along with switches S2, S3, S4 and S5 are respectively coupled to the linear sensing arrays Va and Vb) to the linear sensing array to sample multiple frames of images of the object generated by the sensing array (e.g. a bright spot at time T1 is sampled on capacitor C1 i.e. A1 and as the bright "spot" moves it is over detector B i.e. A2 and at time T3 an average A1+B1 is output on line 6, col. 3 line 49-col. 4 line 17), wherein for each frame, columns of pixels in the linear sensing array are mapped to respective columns of switched capacitor integrators in the linear integrator array (see figure 1a) and

spatially shifting the mapping from the sensing frames along the predetermined direction to produce a summed signal that sums pixel signals from different pixel locations different frames corresponding common image from a location on object (figure 1a and 2 col. 3 line 49-col. 4 line 42 teach shifting the mapping of the sensing frames from Va to Vb to produce a summed signal A+B).

Pettijohn fails to disclose wherein the linear integrator array of switched-capacitor integrators are arranged in rows and columns respectively equal to rows and columns of said linear sensing array wherein for each frame, pixels in columns of the linear sensing array are

mapped in a one-to-one mapping relationship to switched-capacitor integrators in respective columns in the linear integrator array.

However Aswell teaches voltages V1, V2... Vn that are outputted from a linear or an area array having switched capacitors (e.g. S1, C1 and S2, C2... Sn,Cn) corresponding to each column of the pixel array (col. 2 lines 55-59). It is noted that that pixel voltages V1, V2 for pixels in columns of the linear sensing array are mapped in a one-to-one mapping relationship to switched-capacitor integrators S1, C1 and S2, C2... Sn,Cn in respective columns in the linear integrator array.

Therefore taking the combined teachings of Pettijohn and Aswell, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have to the linear integrator array of switched-capacitor integrators are arranged in rows and columns respectively equal to rows and columns of said linear sensing array wherein for each frame, pixels in columns of the linear sensing array are mapped in a one-to-one mapping relationship to switched-capacitor integrators in respective columns in the linear integrator array in order to have only one capacitance and one switch for each column of the pixel as compared to the system of Pettijohn leading to a reduction in area and reduction of the cost of the system.

[Claim 17]

Pettijohn in view of Aswell fails to teach sampling twice the reset and signal levels (CDS) of a pixel during a frame. However Official Notice is taken of the fact that it is notoriously common to sample twice the reset and signal levels (CDS) of a pixel during a frame in order to reduce noise. Therefore taking the combined teachings of Pettijohn, Aswell and Official Notice, it would be obvious to one skilled in the art at the time of the invention to have been motivated to

have to sample twice the reset and signal levels (CDS) of a pixel during a frame in order to reduce noise. [As applicant has not traversed the old and well known statement above, the use of correlated double sampling (CDS) is taken as admitted prior art. See MPEP 2144.03(c)].

Allowable Subject Matter

8. Claims 1-15, 18 and 19 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K. Aggarwal whose telephone number is (571) 272-7360. The examiner can normally be reached on M-F 9:00AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivek Srivastava can be reached on (571)-272-7304. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

YKA
December 16, 2006

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